Power Integrity for SoCs: Power Planning and Signoff Flows

Power integrity has become a crucial part of the system-on-a-chip (SoC) design flow because power-related issues can affect chip timing and even lead to complete device failure. Specifically, excessive rail voltage drop (“IR drop”) and ground bounce can create timing problems and electromigration which can lead to chip failures.

A design’s power integrity can be assured in two ways: through good power-network planning and synthesis and by accurately analyzing the design to detect problems. These planning and analysis steps should not be regarded as isolated sub-flows, however, because they need to be an integrated part of the overall design flow and comprehended early in the design process.

A good power-grid design and sufficient number of $V_{DD}$ and $V_{SS}$ pads limit the effects of IR voltage drop and other power-related issues. However, determining the feasibility of a power-grid design and the correct number of pads requires early analysis. Unfortunately, this analysis is usually required prior to the availability of basic design data.

To address this dilemma, the power-planning methodology described in this paper enables pre-netlist IR-drop analysis. This paper also describes a rail signoff flow and offers a number of practical suggestions for getting the best results from this type of rail-analysis methodology. While this paper mostly focuses on static-IR drop analysis, the growing importance of dynamic IR-drop analysis should also be considered in the overall SoC power closure.
Power planning overview

Before looking at specific power integrity methods, it is important to understand the basics of power planning. The most basic objective of power planning is to ensure that all on-chip components (blocks, memory, I/O, etc.) have adequate power and ground connections. We use the following terms to describe the basic elements of the power network:

- **Power pads** to supply power to the chip.
- **Power rings** which carry power around the periphery of the die, around a standard cell’s core area, and around individual hard macros. The rings are typically in higher-level routing layers to leave lower layers for signal routing. Note that rings are also generally useful around hierarchical blocks. In some cases, these rings consume more area than the budgets allow, so design teams opt for a uniform global mesh and treat the hierarchical blocks as virtual blocks that have no physical power/ground rings around their peripheries.
- **Power rails** (sometimes called row straps or standard cell preroutes), straps, and trunks are horizontal and vertical wires across the entire die or sections of the die. The horizontal wires are often referred to as rails, while the vertical wires are referred to as straps.

Like the power rings, trunks are typically created in the higher-level routing layers. The rails and straps are usually laid out as a uniformly spaced array and then modified to allow for hard-macro power rings, wiring keepout areas, and other restrictions. The power rails connect the standard cell power pins together and then are extended to the power rings, where they are connected with vias. After the straps and trunks are inserted, they are all tied together using vias and via stacks. Using low-level routing (typically METAL 1), the rails are created only within standard cell placement areas that are not already blocked by hard macro placements or wiring keepouts.

The resistance of the metal in this power distribution network causes steady-state IR drop. By reducing the voltage difference between local power and ground, steady-state IR drop reduces both the speed and noise immunity of the local cells and macros. Further, dynamic IR drop occurs when the simultaneous switching of on-chip components causes a dip or spike in the power/ground grid. The current pulled by simultaneously rising edges leads to a dip in the power grid, while a similar phenomenon on falling edges leads to a voltage spike on the ground grid. These phenomena are sometimes referred to as power bounce and ground bounce, respectively, and they reduce the logic gate noise margins. The resulting functional failures or timing errors are extremely difficult to anticipate with traditional signal integrity and timing analysis.

Electromigration occurs when large current densities cause a flow of metal atoms from the negative- to the positive-biased end of a length of interconnect. This flow can result in catastrophic failures by either creating voids (opens in the metal line) or extrusions (shorts with neighboring metal lines). Electromigration has become a bigger problem as interconnect dimensions shrink, causing current densities to rise. The tall-and-thin aspect ratio of today’s interconnect also adds to this problem.
Electromigration problems in power meshes can be avoided by meeting the maximum current density limits for the process (as documented in foundry layout guidelines). When calculating the metal width required, bear in mind that straps wider than the process slotting size will be slotted at some point in the design process, thus reducing their conductivity.

Based on these factors, it is clear that power planning is becoming a critical part of design planning. Power consumption and special power requirements are among many considerations that dictate the placement of cells in a floorplan. For example, some flash memory has a high-voltage programming input that must be within a certain distance of an I/O pin. Taking care of such requirements first is a good idea.

In fact, developing the power structure early helps avoid many problems in the rest of the design flow, and early, accurate analysis is essential. If analysis is put off until late in the flow and the number of power and ground pads must be increased, for example, the additions may cause the design to become pad limited. Similarly, because power structures consume physical area that affects the floorplan, inserting power structures after floorplanning can force floorplan changes. The power grid topology also affects placement and routing within child blocks and thus should be in place immediately after top-level synthesis and prior to final child-block partitioning.

Floorplanning helps avoid IR drop and electromigration problems through strategies such as placing the most power-hungry blocks near the periphery of the die and preventing concentrations of such blocks in any one area. Even if power consumption were spread evenly over the entire chip when viewed from the block level, IR drop would still be worse in the chip's center due to the length of the wires. IR drop in the center of the chip causes the logic there to run slightly slower, and this effect becomes more important in overall timing as threshold voltages decrease.

Some wires in the mesh carry more current than others, so the current on every wire, junction and via should be calculated. Vias that are not big enough act like fuses, ready to blow when the current is too high, so via arrays should be analyzed for IR, current density and electromigration (as described later in this paper).

Calculating the power dissipation at the block level throughout the design process is important to determine if the design is meeting the specified power budget and to estimate the size of the power grid. Early in the design process, manual calculations or spreadsheets are often used to estimate power; as the RTL matures, design tools can be employed to refine power estimates (± - 30% is a reasonable target). As the RTL migrates to gates and transistors, the power estimates can be further improved. For final power signoff of the floorplan, the actual netlist, the net switching activity corresponding to typical operating scenarios, and annotated parasitics should be used.
Creating the power structures

Recent enhancements to floorplanning tools make it possible to synthesize the power grid based on chip power and voltage drop requirements. Previous versions insert power and ground rings, and the designer must specify their width and spacing. In this case, a good rule of thumb is to assume that each side of the ring must carry a quarter of the design’s current. To get this value, divide the overall power budget by four and convert to current using the core’s primary voltage. The allowed current density for the metal layer(s) used for the rings can then be used to determine the required width. If possible, this width should be limited to avoid the need for metal slotting.

It is a good idea to create power and ground rings around any hard macro to enable orientation independence and eliminate the need for the chip’s power structure to conform to the macro’s power structure. Fortunately, most library vendors are now producing hard macros with internal power and ground rings. This practice improves the quality of the IP and simplifies top-level power grid planning. For any hard macros that do not include rings, the same quarter-current rule of thumb can be used to determine the width of the rings.

Once the power rings have been established, power and ground must be routed to the standard cell rows. Abutment of the cells accomplishes some of the connections. The floorplanner is used to add additional rails aligned with the power rails inside of the standard cells. The lowest horizontal metal layer should be used for these additional rails. Some technologies and/or floorplans make it necessary to insert filler cells temporarily to get a complete grid. After insertion of the rails, the filler cells are removed.

The floorplanner makes the rail spacing consistent with the standard cell height, but the user must specify rail width, most often using network synthesis tools that are aware of the process geometries. With the usual mirrored placement rows and their alternating power and ground rails, the width of the additional rails is larger than the width of the straps within the cells. Typically the rail width and spacing increase at each successively higher metal layer. Wider rails can be used in the lowest metal layers, but they often result in the standard cell rows being spaced further apart and therefore reduce the placement area and signal routability.

The straps and trunks that distribute power across the chip offer designers more flexibility than rings and rails and represent the most important means to address specific IR drop issues. Designers must determine the appropriate spacing, width, and layer of these straps and trunks. Note that it is usually better to use many thin routes, (rather than fewer wide routes), especially in the lowest metal layers, to improve overall routability.
Best practices in power planning

The following suggestions may prove useful for achieving good results in power planning:

**Develop physical heuristics for the power/ground mesh**

To minimize IR drop, begin building the power/ground mesh on the metal layer just above the layer used for standard cell power pin connections. Use multiple metal layers to connect the power and ground pads into the core ring. Assuming the standard cell rails use METAL 1, it is best to use a combination of METAL2, METAL3, and additional higher layer metall straps to improve the current capacity from the pad pins to the core ring. In sub-designs (soft macros), avoid “wrong way” power/ground mesh straps (straps that do not use the preferred routing direction for that level).

As a general rule of thumb when designing the power/ground mesh METAL 2 layer, use a spacing that is roughly 10 times the size of the average standard cell width for the design library. The straps on lower layers normally supply a small local area and thus need not be very wide. If the strap spacing on these lowest layers is kept small, the series resistance to any given standard cell is minimized. In addition, thinner wires that align well with the routing grid improve signal routability. For a 0.13 μm process, for example, a spacing of 50 to 100 μm and a width of about 0.5 μm has worked well. Going up toward the top metal layer, the strap spacing can be gradually increased and the wires widened. To avoid large numbers of via stacks from METAL3 to METAL6, METAL4 straps can be added. In most cases it is best to offset the METAL4 straps from the METAL2 straps to avoid long via stacks, or via “walls”.

All power and ground pads that supply the digital core should use a combination of METAL2 and METAL3 at a minimum for their pins, and METAL4 can be added if other design constraints permit. In general, it is best to have a uniform distribution of power and ground pads. Specific suggestions and rules can usually be obtained from the foundry’s layout guidelines documentation. Note, however, that when low-power cells are located around the periphery of the die, putting power and ground pads near the die corners may provide almost no benefit.

**Understand metal resistance characteristics for the target process**

Check vendor-supplied technology files to determine the resistance of each layer used in the power grid. The resistances for the top-most metal layers are typically different from the resistances of the lower level metals due to their increases thicknesses. Because of this difference, the voltage on the mesh may drop faster in one direction that in the other, producing a non-uniform or “squashed” voltage gradient. This effect is especially noticeable in implementations that use an odd number of metal layers.
Note that the non-uniform voltage gradient is not necessarily a problem, but the potential for problems should be considered when designing the power/ground mesh. To minimize the issue, remember that identical metal densities for all layers used in the power/ground mesh do not always imply a uniform IR drop and electromigration result.

**Power network synthesis**

Traditionally, power trunks and straps have been inserted manually, and this process usually involves some degree of trial and error. Power network analysis (PNA) tools have gone mainstream in terms of usability and accuracy, but designers must still create the straps, run the analysis, and then iterate as necessary until adequate results are achieved. Re-work can take as much time as first-pass implementation.

By providing automated power network synthesis (PNS), JupiterXT relieves many of the difficulties of the manual process. Users fill out a form to specify the necessary structure, including variables such as the maximum allowable voltage drop, the ring widths and layers, and the number of trunks. The tool begins by performing an analysis and synthesis of the power grid, then performs PNA under the hood and displays the results. If the results are acceptable, the user can commit them to the design. If not, the user can rerun the synthesis with refined constraints.

With the many degrees of freedom in constraining JupiterXT, synthesizing power grids can seem like more of an art than a science. Given the differing requirements of each design and vendor, users typically need to explore possibilities until the analysis results look good. The iteration time is short enough to generate a lot of choices quickly.

As an alternative to full PNS, the designer can establish a basic power grid and then use PNA to find regions that require refinement to reduce IR drop. PNS can then be run on these specific regions. In addition, power network synthesis can be used to size an existing power network to meet IR drop constraints, and the tool can resize mesh trunks automatically to accommodate new power requirements. JupiterXT can also perform power pad synthesis, which determines the number of power pads needed to meet voltage drop requirements and where they should be placed.

**Power network analysis**

Whether JupiterXT is used to perform power network synthesis or not, the tool can be used for power network analysis (PNA). Coarse placement and a partial power network are sufficient for PNA. Only a top-level power mesh, without vias, is needed for analysis, and the tool automatically creates virtual straps to model standard cell connections.

The tool can also create virtual pads for what-if analysis. These pads simulate additional power/ground pads in the design and eliminate the need to add real power/ground pads in the floorplan to see their effect on IR drop or electromigration.
All that being said, it is good to bear in mind that a more complete the grid yields a more accurate analysis and better correlation as the design progresses through the flow. While early analysis is good, all rails, straps, rings, trunks, and via structures should be included before the final PNA during floorplanning. Additionally, since the power consumed by a cell depends on the load it drives, be sure the design is global-routed in the floorplanner to achieve best PNA results. Accordingly, floorplanner placement and global-route correlation to the detailed-route tool then becomes important.

**Best practices in PNS/PNA**

In parallel with the power-planing heuristics mentioned earlier, the following principles can help in achieving good PNS/PNA results:

- Use the top two metal layers for power and ground, and use a multi-layer mesh.
- The lowest power/ground layer should be perpendicular to the standard cell power rail and at least two layers above the highest standard cell pin layer. This practice eliminates cell-placement and pin-accessibility issues for cells under the power mesh.
- Be sure the following inputs are defined:
  - Power net name(s)
  - Power supply voltage value
  - Power consumption value for the core of the design
  - Target IR drop
- It is recommend that “Optimize Track Usage” be turned on in JupiterXT. This option can conserve routing tracks next to power/ground routes.
- To further increase/preserve routing resources for signal layers, align even metal layers within the power structure and use stacked vias. Do the same for odd metal layers.

**Rail signoff analysis**

The remaining portion of this paper describes some practical considerations that can help ensure a smooth signoff flow for static rail analysis using AstroRail™. After an overview of the suggested flow, the main focus here is to look at the suggestions for making rail analysis run smoothly.

The signoff flow analyzes IR drop and electromigration in large SoCs and was developed during the design of five complex HDTV SoCs. A primary goal was to keep the flow implementation simple for ease of use across multiple designs and processes. A comprehensive push-button flow was unrealistic due to the complexities of the designs and libraries used. The flow falls somewhere between a reference flow (collection of scripts) and a basic production-quality flow in its implementation.

The flow requires only standard DEF and LEF for physical design and library input. Because the flow is standalone for rail signoff, it works with many third-party place-and-
route tools. To allow fast analysis spins late in the design cycle, the flow setup has two parts: reference library preparation and design library preparation. With this setup approach, users create all reference libraries only once in an SoC project; then fast iterations on the design library creation and subsequent analysis can be done each time design changes are made. Note that some library vendors provide Liberty files for only min and max corners, but it is best to have min, nom, and max corners available to enable more operating-condition (PVT) combinations to be analyzed.

Running the rail signoff flow

The recommendation for the first part of the flow—an average power analysis—is to set variables for $V_{DD}$ at a maximum, worst-case (max) synthesis library, and worst-case (c_worst or max_c) signal net parasitics.

A clock-domain-based toggle method can be used with this flow. For example, all signal nets in the target domain can be set to toggle once every other clock, for an equivalent 50 percent toggle rate. A simpler alternative invokes AstroRail’s `poConvertTDF` command to define a 100-MHz clock at the top level and automatically propagate it through the design hierarchy. Then basic switching activity statements can be used:

```plaintext
defineNetSwitchingActivity (geGetEditCell) ".*" 0.04
```

This Astro/AstroRail scheme command sets all signal nets in the design to toggle at a 20 percent toggle rate, as computed using the following equation (in which a toggle consists of two edges per 10 ns clock period):

$$TR = 0.20 \times 2 / 10.0 \text{ ns} = 0.04$$

AstroRail estimates power consumption for hard macros based on the toggle rates of their input ports, but greater accuracy can be obtained by gathering power information from the macro data sheets and annotating it on the hard macros using this simple command:

```plaintext
defineCellInstancePower (geGetEditCell) "Top/A/u1" 1.12e+02
```

After power/ground net extraction come the IR drop and electromigration analyses that are the heart of rail analysis. Experience has shown that two different sets of variables provide the best scenarios for these two analyses. While the IR drop analysis uses worst-case timing conditions (worst parasitics, slow synthesis library, high temperature, and nominal $V_{DD}$), the electromigration analysis requires a hybrid condition (worst parasitics, fast synthesis library, high temperature, highest $V_{DD}$). To determine the worst-case impact on device performance due to the collapsing supply rails, it is useful to modify the recommended IR drop operating conditions: use the worst-case, or lowest, $V_{DD}$.

AstroRail can generate plots of the results of these analyses, and PrimeTime-SI™ can use the instance-based voltage data to determine the delay effects on critical timing paths. Note that the library vendor must support the timing analysis using either k-factors for a
Non-Linear Delay Model (NLDM) library or voltage-drop-aware Scalable Polynomial Delay Model (SPDM) or Composite Current Source (CCS) libraries.

**Rail analysis best practices**

Executing a rail signoff analysis such as the one just described reveals a wide variety of real-world complications—and sometimes not until late in the flow. The following suggestions are intended to help smooth the way to a timely signoff.

**Screen technology and library files**

One of the first steps in the signoff flow is library preparation, and the necessary input files can differ from the ideal in many ways. It is therefore worthwhile to screen the vendor-supplied technology file (.tf) and library LEF used to create the standard cell Milkyway libraries.

First, check the minimum via enclosure and spacing rules defined in the Milkyway technology (.tf) file. These rules need to be modified in many cases so that via arrays in the design DEF properly map to Milkyway contact arrays. Otherwise, opens will occur in the power/ground network. A perl script can be used to modify the minimum grid parameters in the .tf file and ensure the proper minimum enclosure rules.

Second, check the LEF files and verify that each power pad has a “USE POWER ;” attribute defined in each power PIN section and that each ground pad has a “USE GROUND ;” attribute defined in the PIN section. The Milkyway database requires these statements to define the pad cells as power or ground pads for AstroRail.

Third, check the .tf file for information related to electromigration analysis. Search for the keyword “maxCurrDensity” to find the maximum current density values for metals and vias. If the file does not contain these values, they can be defined in the “run configuration” file or manually inside AstroRail. The library vendor’s cell library documentation or user’s guide should contain these values.

Next, check the .tf file for temperature coefficient figures. The file should contain one “temperatureCoeff” keyword/value pair for each metal layer and each via (or contact code, or “cut”) definition. If the file does not contain these values, the user should add the appropriate values as specified in the foundry’s design rule manual and update the library and design technology databases.

Finally, some standard cell LEF files include information such as metal resistance and via resistance, but this information does not always match the presumed “golden” values in the .tf file. Discrepancies can make the analysis inaccurate. An easy way to keep the LEF information from overwriting the .tf information is to have the flow automatically replace the technology file with the properly modified one just after the vendor’s library LEF is read.
Run initial power analyses in “virtual rc” mode

One of the strengths of the AstroRail tool (and, in general, Milkyway tools such as Astro) is that it can analyze a design that has no detailed routing information. The power analysis proceeds with only initial routing estimates.

Using the “virtual rc” mode for extraction, AstroRail completes a quick virtual route prior to running the power analysis. When using this option in design projects, running in “virtual rc” mode produced power estimates and IR drop results within 2 to 5 percent of the results obtained by analyzing an equivalent detail-routed design. In summary, “virtual rc” mode is accurate enough to make early decisions on the power grid while reducing the overall run time.

Start with black-box models, signoff with white-box models

White-box models for hard macros contain only the minimum necessary power and ground network information, but their use can greatly increase chip-level analysis run times for large SoCs if the macro has significant metal slotting or metal fill tracks tied to one or more of the supply rails. In these cases, it can be useful to run analyses with hard macros instantiated as black boxes until the final signoff runs are required.

Check for electromigration violations first

Finding the cause of large IR drop on the power rings can be difficult if only using IR drop analysis, so electromigration plots may be a better place to start. Fixing electromigration violations near the power/ground pads and power rings is relatively easy and tends to clean up the IR drop map, making it easier to evaluate.

The electromigration analysis can also identify places where the power/ground mesh is insufficient or is missing a connection. A hot or warm spot results from wires that are too thin or spaced too far apart and via arrays that have too few vias. It is important to use the initial electromigration analyses to find general weaknesses in the power grid before focusing on detailed electromigration violations. Electromigration violations near the power/ground pads and power rings are relatively easy to find and fix, and these violations have a large effect on the IR drop. Fixing these violations first will clean up the IR drop analysis, making it easier to read and evaluate. To find subtle grid weaknesses, it is useful to “stress” the design by lowering the electromigration violation thresholds or even elevating the analysis voltage above \( V_{DD}\)-max.

Start analysis early

Rough statistical toggle-rate estimates provide a useful starting point for developing and evaluating the power grid. Being a bit pessimistic at the early stages helps reveal power grid weaknesses that would create problems later in the flow. Because changes to the power grid become more difficult after detail-routing, early “what if” power analysis is quite worthwhile. If the clock tree is not yet in the netlist, be sure to account for its power
consumption. The clock tree can consume anywhere from 20 to 50 percent of a design’s dynamic power; this consumption depends on the design architecture, the operating conditions, and the process technology.

Working with rough estimates for toggle rates, AstroRail™ can scale the estimated power to match a user-specified power value using either of the flow’s toggle methods. Spreadsheet estimates usually provide more accuracy by using information such as energy-per-transition and a mapped gate-level netlist to calculate the power. The spreadsheet power estimates can be used in the same way as the rough toggle rate estimates, or the toggle rates can be input to AstroRail and propagated through the logic cones. In fact, running the flow using clock-domain-based switching activity invokes the latter method of power estimation. The AstroRail statistical propagation feature (using PowerCompiler™ technology) analyzes the combinatorial logic functionality to determine the toggle rates for each net and achieves more realistic power estimates even if the toggle rate estimates are somewhat pessimistic.

**Summary: Careful power planning and analysis are essential for 90 nm and below**

Starting power integrity work early is highly worthwhile because it avoids many problems in the later stages of the design flow. The methods described in this paper were developed by Synopsys Professional Services through multiple 90nm implementation projects and offer starting points for power planning as well as analysis. These methodologies can be applied throughout the design flow and serve as a power integrity signoff. Such methods are vital to ensure the performance of today’s SoCs, especially for technology nodes of 90 nm and beyond.